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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/804,051	03/12/2001	Salman Akram	MIO 0069 PA	7513

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EXAMINER
MITCHELL, JAMES M

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 08/01/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/804,051	Applicant(s) AKRAM ET AL.	
	Examiner James Mitchell	Art Unit 2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 February 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This office action is in response to the information disclosure statement filed February 22, 2002.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

3. Claim 1, 4, 5, 8, 25-44 are rejected under 35 U.S.C. 102(e) as being anticipated by Lin (U.S 6,093,969).

4. Lin discloses a multiple die semiconductor assembly comprising: a first semiconductor die (101-1) defining a first active surface arranged is flip chip arranged to an intermediate substrate (103-1), said first active surface including a least one conductive bond pad (101'-1), a second semiconductor die (101-2) defining a second active surface is flip chip arranged to an additional intermediate substrate (103-2), and including a least one conductive bond pad (101'-2) secured to an intermediate substrate (103-1) inherently positioned between said first and second die such that a first surface (bottom) of said substrate faces said first die and a second surface (top) faces said second die, wherein said substrate defines a passage therethrough ("window", 104),

and one of said first die and said second die are positioned such that the conductive bond pads on one of said first and second active surfaces is aligned with said passage, wherein said first and second die is electrically coupled to said intermediate substrate by at least one topographic contact ("wire", 104') extending from said surface (first or second) of said die(first or second) to said first or second surface of said intermediate substrate, and a topographic contact (130-1) conductively coupled to said first die and a topographic contact (130-2) conductively coupled to a said second die; an additional intermediate substrate (130-2) positioned such that a first surface (top) of said substrate faces said second active surface of said second semiconductor die, wherein the additional substrate defines an additional passage therethrough (104-2), said second die is secured ("adhesive", 102-2) to said first surface of said additional substrate such that the conductive bond pad of said second die is aligned with said additional passage, said second die is electrically coupled to said additional substrate by at least one conductive line ("wire") extending from said conductive bond pad through a portion of said passage defined in said additional substrate and to a conductive contact (pad; connecting to 130-2) on a second surface of said additional substrate; and conductive lines (106-1) extending form bond pads on active surface to conductive contacts on said second surface of said intermediate substrate; wherein the first and second die are inherently electrically coupled via being inherently coupled to the first and second intermediate substrate; an encapsulant (104-2) made of an underfill material formed over said first surface of said first intermediate substrate and an encapsulant (104-1) and made of an underfill material formed over and between said first die and a first

surface of first intermediate substrate; wherein topographic contact (130 defines a space between said first active surface and said first surface of said first intermediate substrate.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claim 2, 6, 7, 9, 45, 46-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin in combination with Shoichi (JP 02-158147).

8. Lin discloses the elements stated in paragraph 4.

9. Lin does not appear to disclose a decoupling capacitor or a plurality of decoupling capacitors conductively coupled to at least one of said first and second semiconductor dies, wherein a thickness dimension of said decoupling capacitor is

accommodated in a space defined by a thickness dimension of one of said first and second semiconductor, or a topographic contact extending from an active surface.

10. However Shoichi (2a, 3a) utilizes a decoupling coupled to at least one of said first and second semiconductor dies, wherein a thickness dimension of said decoupling capacitor is accommodated in a space defined by a thickness dimension of one of said first and second semiconductor, or a topographic contact extending from an active surface.

11. It would have been obvious to one of ordinary skill in the art to incorporate a capacitor in the package of Lin such that the capacitor is conductively coupled to a semiconductor die, wherein a thickness dimension (a Y plane) of said decoupling capacitor is accommodated in a space defined by a thickness dimension (a Y plane) of said semiconductor die or a topographic contact, in order to remove noise as taught by Shoichi (Abstract).

12. In regards to clam 47, the prior art discloses the claimed invention except for a plurality of capacitors.

13. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a plurality of capacitors, since it has been held that mere duplication of the essential working components of a device involves only routine skill in the art. *In re Japikse*, 86 USPQ 70 (CCPA 1950).

14. Claim 3 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin in combination with Shoichi and Toy et al. (U.S 5,982,038).

15. Lin and Shoichi disclose the elements in paragraphs 4 and 9-11 and an inherent mounting zone (any area which can be used for mounting) on a substrate defined by lateral dimensions that extends beyond a periphery of at least one of said semiconductor dies.

16. Neither Lin or Shouchi appear to show a heat sink including a cap portion and a peripheral portion nor that the heat sink structure engages a mounting zone on said substrate.

17. However, Toy (Fig 1) utilizes a heat sink (36) including a cap portion (20) inherently thermally coupled to a die (direct contact to die), and a peripheral portion (23) engages an inherent mounting zone mounting defined by a lateral dimension of a substrate.

18. It would have been obvious to one of ordinary skill in the art to incorporate a heat sink including a cap portion and a peripheral portion on a chip package to the modified package of Lin and Shouchi, in order to enhance environmental protection and disperse heat as taught by Toy (Abstract & Column 5, Lines 35-36).

19. Claims 10,13, 14, 17, 20, 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin in view of Lin' 423 (U.S 5,247,423).

20. Lin disclose the elements stated in paragraph 4 and further a method of stacking a plurality of semiconductor die, but does not appear to explicitly disclose that the modules are mounted on a printed circuit board (PCB) wherein the surface of the board faces an intermediate substrate.

21. However, Lin' 423 (Fig 5) utilizes a modules mounted on a PCB wherein the surface of the board is inherently positioned such that it faces an intermediate substrate.

22. It would have been obvious to one of ordinary skill in the art to form the modules of Lin on a printed circuit board (PCB) wherein a first surface of the board faces the intermediate substrate such that topographic contacts extend from a second surface of an intermediate substrate to the first surface of the printed board, in order to make a final circuit as taught by Lin'423 (Column 1, Lines 35-36).

23. With respect to claim 20, the recitation of "a computer system comprising a programmable controller and at least one memory unit, wherein said memory unit comprises a printed circuit board assembly," has not been given patentable weight because it has been held that a preamble is denied the effect of a limitation where the claim following the preamble is a self contained description of the structure not depending for completeness upon the introductory clause. *Kropa v. Robie*, 88 USPQ 478 (CCPA 1951).

24. Claims 11, 15, 16, 18, 21 and 49-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin and Lin' 423 (U.S 5,247,423) in combination with Shoichi.

25. Lin and Lin' 423 disclose the elements stated in paragraphs 18-20, wherein the PCB is a third substrate.

26. Lin does not appear to disclose a decoupling capacitor conductively coupled to at least one of said first and second semiconductor dies, wherein a thickness dimension of said decoupling capacitor is accommodated in a space defined by a thickness

dimension of one of said first and second semiconductor, or a topographic contact extending from an active surface.

27. However Shoichi (2a, 3a) utilizes a decoupling coupled to at least one of said first and second semiconductor dies, wherein a thickness dimension of said decoupling capacitor is accommodated in a space defined by a thickness dimension of one of said first and second semiconductor, or a topographic contact extending from an active surface.

28. It would have been obvious to one of ordinary skill in the art to incorporate a capacitor in the package of Lin such that the capacitor is conductively coupled to a semiconductor die, wherein a thickness dimension (a Y plane) of said decoupling capacitor is accommodated in a space defined by a thickness dimension (a Y plane) of said semiconductor die or a topographic contact, in order to remove noise as taught by Shoichi (Abstract).

29. With respect to claim 21, see paragraph 23.

30. With respect to claim 53, see paragraph 13.

31. Claims 12, 19 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin and Lin' 423 in combination with Shoichi and Toy.

32. Lin, Lin '423 and Shoichi disclose the elements in paragraphs 25-28 and an inherent mounting zone (any area which can be used for mounting) on a substrate defined by lateral dimensions that extends beyond a periphery of at least one of said semiconductor dies.

33. Neither Lin or Shoichi appear to show a heat sink including a cap portion thermally coupled to a major surface of at least one said first and second chip, and a peripheral portion or that the heat sink structure engages a mounting zone on said substrate.

34. However, Toy (Fig 1) utilizes a heat sink (36) including a cap portion (20) thermally coupled to a die (direct contact), and a peripheral portion (23) engages an inherent mounting zone mounting defined by a lateral dimension of a substrate.

35. It would have been obvious to one of ordinary skill in the art to incorporate a heat sink including a cap portion and a peripheral portion on a chip package to the modified package of Lin and Shoichi, in order to enhance environmental protection and disperse heat as taught by Toy (Abstract & Column 5, Lines 35-36).

36. With respect to claim 22, see paragraph 23.

Conclusion

37. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Mitchell whose telephone number is (703) 305-0244. The examiner can normally be reached on M-F 10:30-8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on (703) 305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 305-3230 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

jmm
July 25, 2002

DAVID E. GRAYBILL
PRIMARY EXAMINER